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Function Description TTL I/O

APCIe-1711, CPCIs-1711 and APCI-1710

Multifunction counter board, optically isolated



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Warning!

The following risks result from the improper implementation of the board and from use contrary to the regulations:



Personal injury



Damage to the board, the PC and peripherals



Pollution of the environment.

- Protect yourself, others and the environment!
- Read the safety precautions (yellow leaflet) carefully!

 If this leaflet is not enclosed with the documentation, please contact us and ask for it.
- Observe the instructions of this manual!
 Make sure that you do not forget or skip any step!
 We are not liable for damages resulting from the wrong use of the board.
- Pay attention to the following symbols:



NOTICE!

Designates hints and other useful information.



NOTICE!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed**.



WARNING!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed** and persons may be **endangered**.



Contents

Warn	iing!	3
Chapt	ter overview	5
1	Function description	6
1.1	Board versions with "TTL I/O" function	6
1.2	Block diagram	7
1.3	Used signals	7
1.4	Pin assignment	8
1.5	Connecting the accessories (cables and screw terminal panel)	11
1.6	Connection example	13
2	Standard software	14
3	Technical data and limit values	15
3.1	Digital inputs and outputs (50-pin header)	15
4	Appendix	16
4.1	Index	16
5	Contact and support	17
Figu	ıres	
Fig. 1-		7
Fig. 1-	· ·	
Fig. 1-	· · · · · · · · · · · · · · · · · · ·	
Fig. 1-	•	
Fig. 1-	<u> </u>	
Fig. 1-	<u> </u>	
i ig. I	-0. Connection example	13
Tab	les	
Table	1-1: Used signals	7
Table	1-2: Pin assignment: 50-pin D-Sub male connector and 50-pin header	9



Chapter overview TTL I/O

Chapter overview

In this manual, you will find the following information:

Chapter	Content	
1	Function description including block diagram and pin assignment	
2	Standard software: Information on the API software functions	
3	List of technical data and limit values	
4	Appendix with index	
5	Contact and support address	

This document solely describes the function "TTL I/O".

For general information on the APCIe-/CPCIs-1711 or APCI-1710, please read the respective Technical Description of these boards (see PDF links). It contains, for example, the chapter "Inserting and installing the board" that supports you in commissioning.



1 Function description

Via the 50-pin header, TTL signals can be connected to the board.



NOTICE!

In case other signals are connected, these have to correspond to the TTL level to prevent the board from being damaged.

Please also note that the ports are not optically isolated and that the

Signals PA0 to PA7, PB0 to PB7 and PC0 to PC7 are connected in parallel to all four function modules of the board. To avoid malfunction, the "TTL I/O" function can be loaded only in one function module.

board may be destroyed due to external voltage peaks!

Features:

- For each function module 3 ports (A, B, C) with 8 digital inputs/outputs each (set as inputs after the reset)
- For each function module 1 Port (D) with 2 digital inputs/outputs (set as outputs after the reset)

1.1 Board versions with "TTL I/O" function



NOTICE!

The "TTL I/O" function can be used with every version of the APCIe-1711, CPCIs-1711 or APCI-1710.

The I/O specifications of the different board versions are available in the Technical Description of the APCIe-/CPCIs-1711 or APCI-1710 (see PDF links).



1.2 Block diagram

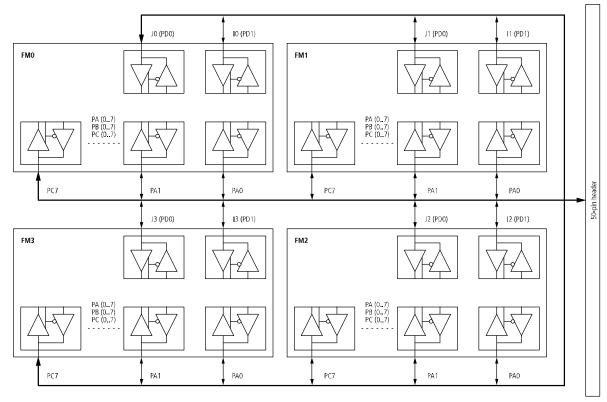


Fig. 1-1: Block diagram: "TTL I/O" function

1.3 Used signals

Ports A, B and C of each function module (FM0 to FM3) each have eight inputs and outputs. In addition, each function module has two inputs and outputs (I and J) of port D, which can only be used for the "TTL I/O" function.

Pin name Signal type **Function** PA0 to PA7 TTL Input or output (after the reset: input) PB0 to PB7 TTL Input or output (after the reset: input) PC0 to PC7 TTL Input or output (after the reset: input) **GND** PC GND GND, not optically isolated Κx TTL Please do not connect anything! Ix (PD0) TTL Input or output (after the reset: output) Jx (PD1) TTL Input or output (after the reset: output)

Table 1-1: Used signals



Pin name	Signal type	Function
V. ext	PC +3.3 V (APCIe-/CPCIs-1711) PC +5 V (APCI-1710)	Voltage supply

x = Number of the function module (0-3)

1.4 Pin assignment

Fig. 1-2: Pin assignment: 50-pin header and 50-pin D-Sub male connector

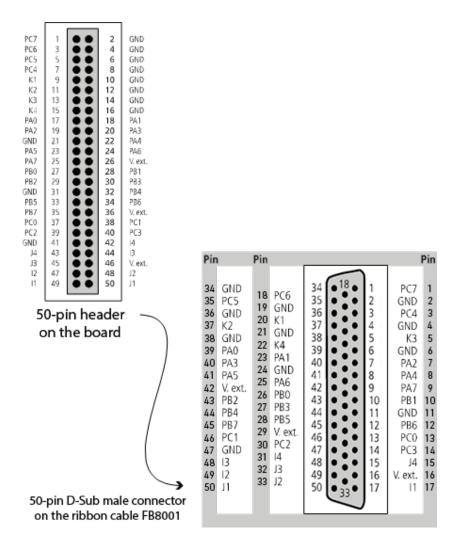




Table 1-2: Pin assignment: 50-pin D-Sub male connector and 50-pin header

	FB8001	Board
Pin name	Pin No. (50-pin D-Sub male connector)	Pin No. (50-pin header)
GND	2	2
GND	4	1
GND	6	5
GND	1	1
GND	1	9
GND	2	1
GND	2	4
GND	3	4
GND	3	6
GND	3	8
GND	47	
I1 ²	1	7
12 ²	4	9
13 ²	42 31 12 50 22 33 32 32	
14 ²		
J1 ²		
J2 ²		
J3 ²		
J4 ²		
K1	20	
K2	37	
К3	5	
K4	22	
PA0	39	
PA1	23	
PA2	7	
PA3	40	
PA4 8		3



Pin name	Pin No. (50-pin D-Sub male connector)	Pin No. (50-pin header)
PA5	4	1
PA6	2	5
PA7	g)
PB0	2	6
PB1	1	0
PB2	4	3
PB3	2	7
PB4	4	4
PB5	2	8
PB6	1	2
PB7	4	5
PC0	1	3
PC1	4	6
PC2	3	0
PC3	1	4
PC4	3	3
PC5	3	5
PC6	1	8
PC7 ¹	1	L
V. ext.	4	2
V. ext.	2	9
V. ext.	1	6

1: PA, PB and PC: Pull-up resistor to 3.3 V (APCIe-/CPCIs-1711) or 5 V (APCI-1710)

2: PD: Serial resistor 100 $\boldsymbol{\Omega}$



1.5 Connecting the accessories (cables and screw terminal panel)

Fig. 1-3: APCIe-1711: Connecting the accessories

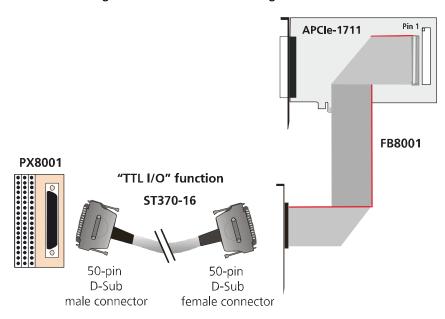
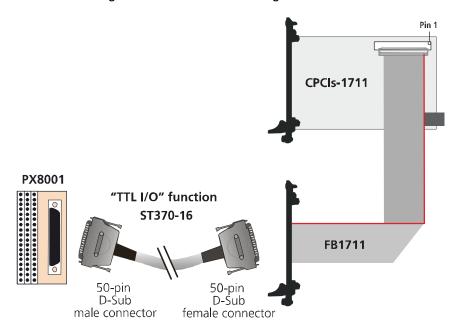


Fig. 1-4: CPCIs-1711: Connecting the accessories





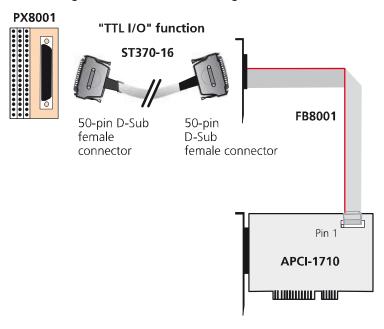


Fig. 1-5: APCI-1710: Connecting the accessories



NOTICE!

Plug the **FB8001** or **FB1711** cable into the connector by inserting the red (or blue or black) cable lead into pin 1.



1.6 Connection example

Pin header FB8001 ST370-16 PX8001 **Board** 47 kΩ 1/6 HC14 1 PC7 29 36 36 29 TTL 9 9 20 20 K1 100 Ω 49 17 49 17 2 2 34 34 GND GND

Fig. 1-6: Connection example

Ports A, B and C are each set to V_{CC} via a pull-up resistor (47 k Ω).



2 Standard software

The API software functions supported by the board are listed in an HTML document. A description of how to access the respective file can be found in the document "Quick installation PC boards" (see PDF link), in the chapter "Standard software".



3 Technical data and limit values

3.1 Digital inputs and outputs (50-pin header)



NOTICE!

The TTL inputs and outputs are not optically isolated.

Please make sure that no signal from the peripherals is connected to the inputs and outputs when the PC system is switched off or being booted up or shut down. This can be realised by means of a relay or tri-state circuit between the peripherals and the TTL inputs and outputs. Moreover, the TTL outputs must be protected against short-circuit through the connected signals.

APCIe-1711, CPCIs-1711

Max. input voltage:	4 V (PC supply voltage = 3.3 V ± 5%)	
Max. output current:	40 mA (no short-circuit protection)	
Signal thresholds:		
Input logic 1:	1.7 V min.	
Input logic 0:	0.8 V max.	
Output logic 1:	2.4 V min. (PC supply voltage ≥ 3 V)	
Output logic 0:	0.45 V max. (PC supply voltage ≥ 3 V)	

APCI-1710

Max. input voltage:	4.75 V (PC supply voltage = 5 V ± 5%)	
Max. output current:	25 mA (no short-circuit protection)	
Signal thresholds:		
Input logic 1:	2 V min.	
Input logic 0:	0.8 V max.	
Output logic 1:	2.4 V min. (PC supply voltage ≥ 4.75 V)	
Output logic 0:	0.45 V max. (PC supply voltage ≥ 4.75 V)	



4 Appendix

4.1 Index

Accessories
Connection 11
Block diagram 7
Board versions 6
Connection example 13
Features 6

Pin assignment 8 Signals 7 Standard software 14 Technical data 15



5 Contact and support

Do you have any questions? Write or call us:

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